Claims:

1. A memory access system comprising:

a controller;

a memory site;

a memory signal transmission path, the memory signal transmission path having a first end and a second end with the first end being connected to the controller and the second end being connected to the memory site;

a memory expansion board connected to the memory site and the memory expansion board being populated with a plurality of modules, each of which modules is comprised of:

a first flex circuit having first and second conductive layers between which conductive layers is an intermediate layer, the first and second conductive layers being interior to first and second outer layers of the first flex circuit, the second conductive layer having upper and lower flex contacts, the upper flex contacts being accessible through second windows through the second outer layer and the lower flex contacts being accessible through first windows through the first outer layer, the first conductive layer and the intermediate layer, the lower flex contacts being further accessible through module contact windows through the second outer layer;

a second flex circuit having first and second conductive layers between which conductive layers is an intermediate layer, the first and second conductive layers being interior to first and second outer layers of the second flex circuit, the second conductive layer having upper and lower flex contacts, the upper flex contacts being accessible through second windows through the second outer layer and the lower flex contacts being accessible through first windows through the first outer layer and the first conductive layer and the intermediate layer, the lower flex

contacts being further accessible through module contact windows through the second outer layer;

a first integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the first integrated circuit connected to the lower flex contacts of the first and second flex circuits;

a second integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the second integrated circuit connected to the upper flex contacts of the first and second flex circuits, the first and second flex circuits being disposed about the first and second lateral sides, respectively, of the first integrated circuit to place the upper flex contacts of the first and second flex circuits between the first and second integrated circuits; and

a set of module contacts.

2. The memory access system of claim 1 in which the memory signal transmission path is comprised of an address and command transmission path and a data transmission path.

3. The memory access system of claim 1 in which the memory expansion board is a DIMM.

4. The memory access system of claim 1 further comprising:

a third integrated circuit; and

a fourth integrated circuit.

5. The memory access system of claim 4 in which the first, second, third, and fourth integrated circuits in each of the plurality of modules are separately accessed.

6. A memory access system comprising:

a controller;

a memory site;

a memory signal transmission path, the memory signal transmission path having a first end and a second end with the first end being connected to the controller and the second end being connected to the memory site;

a memory expansion board connected to the memory site and the memory expansion board being populated with a plurality of modules, each of which modules is comprised of:

flex circuitry having first and second conductive layers, the second conductive layer having upper and lower flex contacts;

a first integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the first integrated circuit connected to the lower flex contacts of the flex circuitry;

a second integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the second integrated circuit connected to the upper flex contacts of the flex circuitry, the flex circuitry being disposed to place the upper flex contacts of the flex circuitry between the first and second integrated circuits.

7. The memory access system of claim 6 in which the second conductive layer of the flex circuitry comprises at least one demarked voltage plane and a voltage set of the upper flex contacts and a voltage set of the lower flex contacts connect

voltage conductive contacts of the first and second integrated circuits to one of the at least one voltage planes.

8. The memory access system of claim 6 in which each of the plurality of modules further comprises at least one form standard.

9. The memory access system of claim 6 further comprising:

a third integrated circuit; and

a fourth integrated circuit.

10. The memory access system of claim 9 in which the first, second, third, and fourth integrated circuits in each of the modules of the plurality of modules are separately accessed.

11. A memory access system comprising:

a controller;

a memory site;

a memory signal transmission path, the memory signal transmission path having a first end and a second end with the first end being connected to the controller and the second end being connected to the memory site;

a memory expansion board connected to the memory site and the memory expansion board being populated with a plurality of modules, each of which modules is comprised of:

first flex circuitry;

second flex circuitry;

third flex circuitry;

a first integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the first integrated circuit connected to the first flex circuitry;

a second integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the second integrated circuit connected to the second flex circuitry;

a third integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the third integrated circuit connected to the third flex circuitry; and

a fourth integrated circuit having first and second lateral sides and upper and lower major surfaces with contacts along the lower major surface, the contacts of the fourth integrated circuit connected to the third flex circuitry, the first, second, third, and fourth integrated circuits being disposed in a stacked relationship.

12. The memory access system of claim 11 in which the first flex circuitry, the second flex circuitry, and the third flex circuitry each are comprised of two conductive layers.

13. The memory access system of claim 11 in which the first, second, third, and fourth integrated circuits in each of the plurality of modules are separately accessed.

14. A memory access system comprising:

a controller;

a memory site;

a memory signal transmission path, the memory signal transmission path having a first end and a second end with the first end being connected to the

controller and the second end being connected to the memory site and there being no memory connected to the memory signal transmission path other than through the memory site;

a single memory expansion board connected to the memory site and the memory expansion board being populated with a plurality of modules, each of which modules is comprised of:

a first CSP;

a second CSP;

a third CSP;

a fourth CSP, all of which CSPs are in a stacked arrangement, one above the other.

15. The memory access system of claim 14 in which the memory expansion board is a DIMM populated with 18 modules.

16. The memory access system of claim 14 in which a first form standard is disposed between the first and second CSPs and a second form standard is disposed between the second and third CSPs and a third form standard is disposed between the third and fourth CSPs

17. The memory access system of claim 14 in which the first, second, third, and fourth CSPs in each of the plurality of modules are separately accessed.

18. A memory access system comprising:

a controller;

a memory site;

a memory signal transmission path, the memory signal transmission path having a first end and a second end with the first end being connected to the controller and the second end being connected to the memory site;

a memory expansion board connected to the memory site and the memory expansion board being populated with a plurality of modules, each of which modules is comprised of:

a first CSP having an upper surface and a lower surface and a body with a height H1 that is the shortest distance from the upper surface to the lower surface of the first CSP, and along the lower surface there are plural first CSP low profile contacts, each of which plural first CSP low profile contacts extends no more than 7 mils from the surface of the first CSP;

a second CSP in stacked disposition with the first CSP, the second CSP having an upper surface and a lower surface and a body with a height H2 that is the shortest distance from the upper surface to the lower surface of the second CSP, and along the lower surface there are plural second CSP low profile contacts, each of which plural second CSP low profile contacts extends no more than 7 mils from the surface of the second CSP;

a first flex circuitry that connects the first CSP and the second CSP, a portion of which flex circuitry is disposed between the first and second CSPs.

19. The memory access system of claim 18 in which the plural first CSP low profile contacts and the plural second CSP low profile contacts are HT joints.

20. The memory access system of claim 18 in which plural module contacts are disposed along the first flex circuitry.

21. The memory access system of claim 18 in which the shortest distance from the lower surface of the second CSP to the upper surface of the first CSP that passes through one of the plural second CSP low profile contacts is less than 11 mils.

22. The memory access system of claim 18 in which the first flex circuitry is comprised of two flex circuits, each of which flex circuits has two conductive layers.

23. The memory access system of claim 18 in which the shortest distance from the lower surface of the second CSP to the upper surface of the first CSP that passes through one of the plural second CSP low profile contacts is no more than 9 mils.

24. The memory access system of claim 18 in which the first flex circuitry is comprised of two flex circuits, each of which flex circuits has one conductive layer.

25. The memory access system of claim 18 further comprising a form standard disposed above the upper surface of the first CSP.

26. The memory access system of claim 25 in which the shortest distance from the lower surface of the second CSP to the upper surface of the first CSP that passes through one of the plural second CSP low profile contacts is no more than 17 mils.

27. The memory access system of claim 18 further comprising:

a first form standard disposed above the upper surface of the first CSP; and

the first flex circuitry is comprised of two flex circuits, each of which flex circuits has two conductive layers at least one of which conductive layers has plural flex contacts and in which the shortest distance from the lower surface of the second CSP to the upper surface of the first CSP that passes through one of the plural second CSP low profile contacts is no more than 17 mils

28. The memory access system of claim 27 in which the plural first CSP low profile contacts and the plural second CSP low profile contacts are HT joints, selected ones of which HT joints are in contact with flex contacts of the first flex circuitry.

29. The memory access system of claim 18 further comprising:

a third CSP having an upper surface and a lower surface and a body with a height H3 that is the shortest distance from the upper surface to the lower surface, and along the lower surface there are plural third CSP low profile contacts, each of which plural third CSP low profile contacts extends no more than 7 mils from the surface of the third CSP;

a fourth CSP in stacked disposition with the third CSP, the fourth CSP having an upper surface and a lower surface and a body with a height H4 that is the shortest distance from the upper surface to the lower surface, and along the lower surface there are plural fourth CSP low profile contacts, each of which plural fourth CSP low profile contacts extends no more than 7 mils from the surface of the fourth CSP, the third CSP being disposed above the second CSP and the fourth CSP being disposed above the third CSP; and

a second flex circuitry connecting the second CSP and the third CSP; and

a third flex circuitry connecting the third CSP and the fourth CSP.

30. The memory access system of claim 29 in which the first, second, third, and fourth CSPs in each of the modules of the plurality of modules are separately accessed.

31. The memory access system of claim 29 in which the first CSP is disposed beneath the second CSP and the shortest distance from the upper surface of the fourth CSP to the lower surface of the first CSP that passes through at least one of the plural fourth CSP low profile contacts is less than HEIGHT where HEIGHT = 45 mils + H1 + H2 + H3 + H4.

32. The memory access system of claim 29 further comprising first, second and third form standards each respectively disposed above the upper surface of the first, second, and third CSPs.

33. The high-density circuit module of claim 32 in which the shortest distance from the upper surface of the fourth CSP to the lower surface of the first CSP that passes through at least one of the plural fourth CSP low profile contacts is less than HEIGHTFS where HEIGHTFS = 65 mils + H1 + H2 + H3 + H4.

34. The high-density circuit module of claim 18 further comprising:

a third CSP having an upper surface and a lower surface and a body with a height H3 that is the shortest distance from the upper surface to the lower surface, and along the lower surface there are plural third CSP low profile contacts, each of which plural third CSP low profile contacts extends no more than 7 mils from the surface of the third CSP;

a fourth CSP in stacked disposition with the third CSP, the fourth CSP having an upper surface and a lower surface and a body with a height H4 that is the shortest distance from the upper surface to the lower surface, and along the lower surface there are plural fourth CSP low profile contacts, each of which plural fourth CSP low profile contacts extends no more than 7 mils from the surface of the fourth CSP, the third CSP being disposed above the second CSP and the fourth CSP being disposed above the third CSP; and

a second flex circuitry connecting the second CSP and the third CSP, the second flex circuitry being comprised of two conductive layers at least one of which two conductive layers has plural flex contacts; and

a third flex circuitry connecting the third CSP and the fourth CSP, the second flex circuitry being comprised of two conductive layers at least one of which two conductive layers has plural flex contacts; and

second and third form standards respectively disposed above the second and third CSPs.

35. The memory access system of claim 34 in which at least one of the flex contacts has an orifice.

36. The memory access system of claim 34 in which the first, second, and third form standards are comprised of copper.

37. The memory access system of claim 34 in which the shortest distance from the lower surface of the fourth CSP to the upper surface of the first CSP that passes through one of the plural fourth CSP low profile contacts is less than HEIGHT4 where HEIGHT4 = 65 mils + H1 + H2 + H3 + H4.

38. The memory access system of claim 34 in which the first, second, third, and fourth CSPs in each of the plurality of modules are separately accessed.

39. A memory access system comprising:

a controller;

a memory expansion board, the memory expansion board being populated with a plurality of modules, each of which modules comprising:

a first CSP;

a second CSP, the second CSP being disposed above the first CSP;

flex circuitry connecting the first CSP and the second CSP, the flex circuitry having plural flex contacts of which at least one has an orifice that has a median opening extent of DO; and

plural consolidated contacts, a selected one of which passes through the orifice and the selected one of the plural consolidated contacts having an inner flex portion and an outer flex portion delineated by the orifice, the selected one of the plural consolidated contacts providing a connection between the first CSP and the flex circuitry and the outer flex portion of the selected one of the plural consolidated contacts having a median lateral extent of DCC and DCC is larger than DO; and

a memory signal transmission path having a first end connected to the controller and a second end connected to the memory expansion board and there being no other memory connected to the transmission path other than that with which the memory expansion board is populated.

40. The memory access system of claim 39 further comprising in each of the plurality of modules with which the memory expansion board is populated:

a third CSP; and

a fourth CSP.

41. The memory access system of claim 40 in which the first, second, third, and fourth CSPs in each of the plurality of modules are accessed individually.